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| EXAMINER | |
|---|---|
| PATEL, KAUSHIKKUMAR M | |
| **ART UNIT** | **PAPER NUMBER** |
| 2188 | |

DATE MAILED: 09/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/922,153 | MORAN, DOV | |
| | Examiner | Art Unit | |
| | Kaushikkumar Patel | 2188 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *10 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *19, 22-28 and 36-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *19, 22-28 and 36-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Response to Amendment*

1. This Office Action is in response to applicant's communication filed July 10, 2006 in response to PTO Office Action mailed May 19, 2006. The Applicant's remarks and amendments to the claims and/or the specification were considered with the results that follow.

2. In response to the last Office Action, no claims have been amended. Claims 1-18, 20-21 and 29-35 have been canceled. Claim 37 has been added. As a result, claims 19, 22-28 and 36-37 are now pending in this application.

### *Response to Arguments*

3. Applicant's argument with respect to Garfunkel's flash memory being directly executable is persuasive.

4. Applicant's arguments with respect to claims 19, 22-28 and 36-37 have been considered but are moot in view of the new ground(s) of rejection.

### *Claim Objections*

5. Claim 25 is objected to because of the following informalities: Acronyms (such as CPU in claim 25) should not be used to abbreviate key terms until they are explicitly defined previously within the claim or a claim to which it depends from. An acceptable

correction would be for example in claim 25, "central processing unit (CPU)".

Appropriate correction is required.

***Double Patenting***

6. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

7. Claims 19 and 22-28 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-2 of copending Application No. 10/888012.

This is a provisional obviousness-type double patenting rejection since the conflicting claims have not in fact been patented.

***Claim Rejections - 35 USC § 112***

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

9. Claims 22 and 23 are rejected under 35 U.S.C. 112, second paragraph as being indefinite.

10. Claim 22 recites the limitation "the code" in line 9. There is insufficient antecedent basis for this limitation in the claim.

Claim 23 recites the limitations "a second portion" and "the code" in line 2. There is insufficient antecedent basis for these limitations in the claim.

11. Claim 28 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 28 recites limitation "the flash memory being of a type such that the external processor cannot read boot code to be executed directly from said flash memory" is unclear. According to broadest reasonable interpretation means that processor cannot read any data directly from flash memory at any time, since boot code is a type of data stored in the flash memory. Accordingly, it is understood that "processor cannot execute the boot code to be executed, directly from said flash memory" in this office action.

***Claim Rejections - 35 USC § 103***

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claims 19, 24-27 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gefen et al (US PUB 2002/0138702) and further in view of Applicant's Admitted Prior Art (AAPA herein after).

As per claim 19, Gefen discloses a method for executing (booting) a (system) code [par. 22, although Gafen explicitly not teaching a boot code, but the phrase "*the code to be executed*" includes any program code that can be executed by the processor, see AAPA par. 3, such executable code is required for running software programs and, for "booting" the computational device], the system featuring a processor for executing (boot) code (par. 27), the method comprising:

providing a flash based unit in the system for storing the boot code to be executed [*NAND Flash 14; Fig. 1*], said flash-based unit comprising a flash memory of a restricted type, being characterized in that code cannot be directly executed from said flash memory [*NAND Flash is not executable*; Paragraph 8], and a volatile memory component for receiving a portion of the boot code to be executed [*SRAM memory 10 and SRAM buffer 20*; Figs. 1 and 2, (par. 32), *the data inside the SRAM 10 is a copy of a portion of the NAND flash 14 content*];

sending a busy signal to said processor (Paragraphs 38, 39);

transferring said portion of the boot code to said volatile memory component [*data from the NAND flash array 14 is downloaded into SRAM 10, such that the data inside the SRAM 10 is a copy of a portion of the NAND flash 14 content;* Par. 32];

removing said busy signal (where it is understood that when memory device is in process of downloading data for execution, it is required to send "busy signal" to executing entity to hold off the execution and once the required data is transferred, the execution can resume by removing the busy signal; Paragraphs 39-40).

However, Gefen does not specifically teach said portion of the boot code being for basic initialization of the system as recited in the claim.

AAPA discloses a portion of the boot code being for basic initialization of the system (*typical "boot" operations include initialization of the hardware components of the computational device and loading of required software programs*, par. 3,); executing said first portion of the boot code by said processor (*contents within SRAM 10 "becomes" executable*; Gefen, par. 32).

Thus, it would have been obvious to one of ordinary skill in the art, at the time of invention by applicant to modify the system of Gefen to include portion of boot code for basic initialization of a system as taught by AAPA, because as evident from AAPA during the system start up all hardware components must be initialized to make it operable (AAPA par. 3) and Since Gefen's system loads a portion of flash memory component into SRAM due to smaller size of executable memory (Gefen, pars. 12-18), one having ordinary skill in the art at the time of the invention would have loaded a first

portion of code to SRAM of Gefen for basic initialization of the system as taught by AAPA above.

As per claims 24-27, Gefen and AAPA disclose the claimed invention as detailed per claim 19 above in the previous paragraphs.

Gefen further discloses a volatile memory is large enough to store portion of the boot code only sufficient for basic initialization of a system (the NAND Flash is 8mB while the SRAM is 1KB, equal or smaller in size to the portion of code in the flash memory; Paragraph 30).

As per claim 36, Gefen discloses a flash-based unit separate from the processor (*flash memory 14 is separate from processor coupled to executable interface*; Figs. 1 and 2).

14. Claims 37 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gefen et al (US PUB 2002/0138702) and further in view of Applicant's Admitted Prior Art (AAPA) as applied to claim 19 above, and further in view of Gibson et al (US 6,601,167).

As per claim 37, Gefen and AAPA teach limitations (including sending busy signal) of claim 19, but fail to teach sending busy signal in response to a power-on signal as recited in the claim. As explained with respect to claim 19, Gefen teaches sending a busy signal to executing entity to notify that the required code is not yet available when data is downloaded from flash to SRAM (par. 40). Gibson teaches that

flash memories are not ready to read immediately (limitation of claim 28, although claim 28, recites processor cannot read boot code directly, it is understood as processor can not read boot code during powering on the computing system) following power being supplied (col. 1, lines 55-62) and hence power on halt signal to processor (col. 3, lines 42-51).

Thus it would have been obvious to one having ordinary skill in the art at the time of the invention to send busy signal to processor during power on as taught by Gibson in the system of Gefen and AAPA to prevent processor from executing instructions when there is no data available (Gibson, col. 3, lines 45-49, and Gefen, par. 40).

15. Claims 22 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gefen et al (US PUB 2002/0138702) and Applicant's Admitted Prior Art (AAPA herein after) (and Gibson US 6,601,167 incorporated as an evidentiary reference).

As per claim 22, Gefen discloses a method for executing (booting) a (system) code [par. 22, although Gafen explicitly not teaching a boot code, but the phrase "*the code to be executed*" includes any program code that can be executed by the processor, see AAPA par. 3, such executable code is required for running software programs and, for "booting" the computational device], the system featuring a processor for executing (boot) code (par. 27), the method comprising:

providing a flash based unit in the system for storing the boot code to be executed [*NAND Flash 14; Fig. 1*], said flash-based unit comprising a flash memory of a

restricted type, being characterized in that code cannot be directly executed from said flash memory [*NAND Flash is not executable*; Paragraph 8], and a volatile memory component for receiving a portion of the boot code to be executed [*SRAM memory 10 and SRAM buffer 20*; Figs. 1 and 2, (par. 32), *the data inside the SRAM 10 is a copy of a portion of the NAND flash 14 content*]; transferring a first portion of boot code to said volatile memory component [*data from the NAND flash array 14 is downloaded into SRAM 10, such that the data inside the SRAM 10 is a copy of a portion of the NAND flash 14 content;* Par. 32];

However, Gefen does not specifically teach said portion of the boot code being for basic initialization of the system as recited in the claim.

AAPA discloses a portion of the boot code being for basic initialization of the system (*typical "boot" operations include initialization of the hardware components of the computational device and loading of required software programs*, par. 3,); executing said first portion of the boot code by said processor (*contents within SRAM 10 "becomes" executable*; Gefen, par. 32).

Thus, it would have been obvious to one of ordinary skill in the art, at the time of invention by applicant to modify the system of Gefen to include portion of boot code for basic initialization of a system as taught by AAPA, because as evident from AAPA during the system start up all hardware components must be initialized to make it operable (AAPA par. 3) and Since Gefen's system loads a portion of flash memory component into SRAM due to smaller size of executable memory (Gefen, pars. 12-18), one having ordinary skill in the art at the time of the invention would have loaded a first portion of code to SRAM of Gefen for basic initialization of the system as taught by AAPA above.

Gefen also fails to teach the first portion of the boot code command for copying a second portion of the boot code. Gefen teaches a downloading algorithm to copy different portions of flash memory to volatile memory that requires monitoring the instructions in SRAM (fig. 2, item 22 and pars. 34-36). The booting process (as evident from AAPA, par. 3) executes in series of steps, such as hardware component initialization and then loading other required software programs and system codes.

Thus, it would have been obvious to one having ordinary skill in the art at the time of the invention to create a boot program in series of steps to copy next portion of code in the volatile memory after finishing executing the portion of code currently residing in the volatile memory (such boot code is known in the art, see Gibson, col. 2, lines 32-34). The motivation to create such type of code would be simpler system implementation and faster code execution.

As per claim 23, Gefen teaches transferring the second portion of code to said volatile memory component (pars.34 and 41).

***Conclusion***

16. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is required under 37 C.F.R. § 1.111(c) to consider these references fully when responding to this action. The documents cited therein teach non-executable flash memory.

17. The examiner requests, in response to this Office action, support be shown for language added to any original claims on amendment and any new claims. That is, indicate support for newly added claim language by specifically pointing to page(s) and line no(s) in the specification and/or drawing figure(s). This will assist the examiner in prosecuting the application.

18. When responding to this office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present, in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections See 37 CFR 1.111(c).

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kaushikkumar Patel whose telephone number is 571-272-5536. The examiner can normally be reached on 8.00 am - 4.30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 571-272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kaushikkumar Patel
Examiner
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